SESSION 9 – TAPA II
Advanced Transistor Technology II

Wednesday, June 16, 8:00 a.m.
Chairpersons: J. Woo, UCLA
H. Wakabayashi, NEC

9.1 — 8:00 a.m.
A hp22 nm Node Low Operating Power (LOP) Technology with Sub-10 nm Gate Length Planar Bulk CMOS Devices, N. Yasutake, K. Ohuchi, M. Fujiwara, K. Adachi, A. Hokazono, K. Kojima, N. Aoki, H. Suto, T. Watanabe, T. Morooka, H. Mizuno, S. Magoshi, T. Shimizu, S. Mori, H. Oguma, T. Sasaki, M. Ohmura, K. Miyano, H. Yamada, H. Tomita, D. Matsushita, K. Muraoka, S. Inaba, M. Takayanagi, K. Ishimaru and H. Ishiuchi, Toshiba Corporation, Kanagawa, Japan

High performance 10 nm gate length CMOSFETs for hp22 nm node LOP is demonstrated for the first time. Key process, such as elevated source/drain extension combined with flash lamp annealing, fully silicided metal gate, novel SiON, and optimization method under high Vdd condition which taking care of SRAM performance is described. Record high transconductance of 1706 mS/mm andover 400 GHz ft is achieved for nMOSFET. Bulk planar MOSFET structure can be extend down to hp22 nm node.

9.2 — 8:25 a.m.
A Simplified Hybrid Orientation Technology (SHOT) for High Performance CMOS, B. Doris, Y. Zhang*, D. Fried, J. Beintner, O. Dokumaci, W. Natzle, H. Zhu, D. Boyd, J. Holt, J. Petrus, J. T. Yates, T. Dyer, P. Saunders*, M. Steen*, E. Nowak and M. Ieong, IBM SRDC, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY

A new concept in high performance VLSI called Simplified Hybrid Orientation Technology (SHOT) is introduced. This novel process flow creates circuits with independently oriented surface channels for pMOS and nMOS by integrating FinFETs with planar Ultra-Thin SOI (UTSOI) MOSFETs for the first time. The unique CMOS structure enables high mobility surface channel orientation for both devices. The SHOT scheme is also capable of producing PDSOI devices on the same chip.

9.3 — 8:50 a.m.
Power-aware 65 nm Node CMOS Technology Using Variable V_{dd} and Back-bias Control with Reliability Consideration for Back-bias Mode, M. Togo, T. Fukai, Y. Nakahara*, S. Koyama*, M. Makabe*, E. Hasegawa*, M. Nagase*, T. Matsuda*, K. Sakamoto*, S. Fujiwara*, Y. Goto*, T. Yamamoto, T. Mogami, M. Ikeda*, Y. Yamagata*, and K. Imai*, NEC Corp., Kanagawa, Japan and *NEC Electronics Corp., Kanagawa, Japan

We have developed a power-aware CMOS technology featuring variable VDD and back-bias control. Three typical operation modes are defined: high-speed mode (VDD=1.2V, VB=0V), nominal mode (VDD=0.9V, VB=-0.5V) and power-save mode (VDD=0.6V, VB=-2.0V). Compared with nominal mode, one and a half order of magnitude reduction of standby leakage current is achieved with power-save mode, while 75% higher drivability is achieved with high-speed mode. Device reliability for back-bias condition was also investigated. With higher back-bias, NBT (Negative Bias Temperature) degradation for pFET is enhanced especially in the case of thinner gate oxide. From activation energy, we believe the dominant mechanism is SHH (Substrate Hot-Hole) injection. Reduced VDD at standby mode drastically alleviates this degradation caused by NBT stress and SHH injection. With appropriate VDD and VB combination, power-aware 65nm CMOS with sufficient reliability can be achieved.

9.4 — 9:15 a.m.
Symmetrical 45nm PMOS on (110) Substrate with Excellent S/D Extension Distribution and Mobility Enhancement, J.R. Hwang, J.H. Ho, Y.C. Liu, J.J. Shen, W.J. Chen, D.F. Chen, W.S. Liao, Y.S. Hsieh, W.M. Lin, C.H. Hsu, H.S. Lin, M.F. Lu, A. Kuo, S. Huang-Lu, H. Tang, D. Chen, W.T. Shiau, K.Y. Liao and S.W. Sun, United Microelectronics Corporation, Hsin-Chu City, Taiwan, ROC

For the first time, 45 nm PMOS devices on the only 4-fold symmetry zone of (110) surface substrates were demonstrated with excellent diffusion control in the S/D extension region. A 30% drive current enhancement was observed compared to devices on conventional (100) substrates with <110> channel. Resistance to gate oxide interface generation induced by charge injection stress is increased by 2 times. Improved 1/f noise characteristics were also observed on (110) surface substrates, especially when devices operate at linear region.

9.5 — 9:40 a.m.
65nm CMOS High Speed, General Purpose and Low Power Transistor Technology for High Volume Foundry Application, S.K.H. Fung, H.T. Huang, S.M. Cheng, K.L. Cheng, S.W. Wang, Y.P. Wang, Y.Y. Yao, C.M. Chu, S.J. Yang, W.J. Liang, Y.K. Leung, C.C. Wu, C.Y. Lin, S.J. Chang, S.Y. Wu, C.F. Nieh, C.C. Chen, T.L. Lee, Y. Jin, S.C. Chen, L.T. Lin, Y.H. Chiu, H.J. Tao, C.Y. Fu, S.M. Jang, K.F. Yu, C.H. Wang, T.C. Ong, Y.C. See, C.H. Diaz, M.S. Liang and Y.C. Sun, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC

This paper presents a state-of-the-art 65nm CMOS transistor technology using 300mm bulk substrate. Device offering is classified as High Speed (HS), General Purpose (G) and Low Power (LP) so as to cover the whole foundry application space with various power and performance requirement. High volume manufacturable 55nm / 45nm and <40nm gate length transistor at EOT 1.95nm /1.4nm and 1.2nm are achieved using thermal cycle reduction together with optimized gate height and gate activation dose. Advantage of Laser Spike Anneal (LSA) over conventional RTA is demonstrated for the first time. NFETpoly depletion is reduced by 1A and drive current is increased by 7%.